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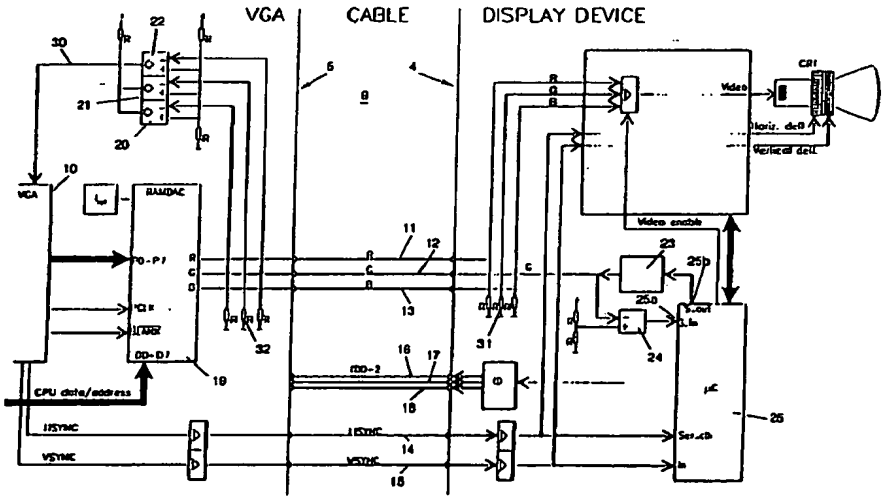

(57) Abstract

The invention relates to a method for controlling a display device in a display system, and to a display system and a display device. In order to achieve a user-friendly display system where the properties of both the display device and the display controller can be utilized as efficiently as possible, a bidirectional data transmission path is established between the display device (4) and the means (5, 1) controlling it so that at least one signal line (12) used for controlling the image displayed by the display device (4) is also utilized in the data transmission mode as the data transmission path.

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A method for controlling a display device in a display system, and a display system and a display device

The invention relates to a method for controlling a display device in a display system, and to a display system and a display device. In the method, data concerning the display device is transmitted from the display device to display control means, and image control data is transmitted from the display control means to the display device for controlling an image displayed by the display device. The display system according to the invention comprises a display device and display control means controlling the display device and connected to the display device by means of at least one signal line intended for controlling an image displayed by the display device, and possibly by means of at least one signal line used for identifying the display device. The display device according to the invention is such as disclosed in the preamble of the attached claim 17.

Video information is transmitted by the display control means to the display device as serial data coupled to the synchronizing signals. The display device receives the serial video information and displays it on the screen in a position determined by the synchronizing signals.

The display devices are generally cathode ray tube (CRT) based devices which have a single deflection frequency and in which the image has been factory-adjusted (e.g. the position of the image on the screen). The most recent display devices are able to synchronize with several deflection frequencies within a predetermined display device specific frequency range (so-called multisync-monitors). The

earliest display devices and display controllers (EGA, CGA, MDA, HGC) of the PC environment employ merely TTL-level signals in the transmission of video information, whereas the most recent devices (VGA, 8514/A, XGA) employ analog video signals so as to create a larger colour/grey scale and to reduce the number of signal conductors. In most cases the synchronizing signals are still transmitted as TTL-level signals or in combination with each other or in combination with the video signals (composite video). Analog transmission usually employs three signals R (red), G (green) and B (blue). In the monochrome environment, only the G signal is used. The levels of the analog video signals indicate directly the intensity of the corresponding pixel to be displayed on the screen. By combining the levels of the analog R, G and B signals, it is possible to produce an innumerable number of different colours for the display device.

For identifying the present-day display devices, the most recent PC equipments utilize separate identification signals (ID signals) the number of which is usually 3 (IBM PS/2 analog monitors), which enables the identification of eight different display devices. At present the VGA-type display controllers do not, however, employ the ID signal identification to any greater extent; they merely distinguish between the monochrome and colour display device on the basis of the different voltage levels of their video signals. In the monochrome and colour display device, the levels of the video signals deviate from each other due to the different matching (termination) of the video signals in the display device.

In high-resolution display devices of higher

quality, so-called BNC video connectors are used, and so the identification signal connection has to be performed in the signal cable to achieve compatibility. In such cases the display device usually uses R, G and B signals (the synchronizing signal combined with the G signal) and possibly a combined horizontal/vertical deflection signal separately, or separate horizontal and vertical deflection signals.

In order that the display device could be used in different display modes, the microcomputer (display controller) has to use certain preselected video parameter tables to describe the different display modes. The user thereby has to be able to pick up the right alternative from the display device menu of the display controller installation program and inform the program about the selection so that the program can select the parameters corresponding to the particular display mode from the tables. One factor making the selection considerably more difficult is the uncertainty about the compatibility of the different display devices; the display controllers usually support only certain most widely used display devices, and the user encounters problems if his display device is not contained in the display device menu of the installation program of the display controller. In order for the microcomputer to be able to support a large number of different display devices, a great number of different video parameter tables has to be created for the display controller, and the storage of such tables requires plenty of memory space and causes thus extra costs.

Another factor hampering the identification of the display device is that only three ID signals are

used in the signal cable, which allows the identification of eight different display devices only. In spite of the ID signals specified by IBM, a great number of display device manufacturers use ID signal combinations that deviate from the specifications, or no such signals are used (the signal lines are left unconnected). This decreases considerably the reliability of the identification of the display device by software. The use of the specified ID signal combinations does not either provide additional information about the additional properties of other so-called compatible display devices (such as the frequency range, resolution, etc.)

A further disadvantage of the present display systems is that the factory adjustments of the display device have to be performed after the manufacturing process; in practice, they are performed manually on the basis of a test image either by altering the set values of the software by a microprocessor-based control, or by altering the values of components, such as adjustable resistors. The adjustments to be performed include determining the position of the image on the screen and the size of the image. In cases where there are several display modes and where part of the adjustments are interdependent, calling for an appropriate "compromise adjustment", the performance of the adjustments requires plenty of time, thus also causing costs.

Further costs are caused by the service of the device, which almost always requires the visit of the service staff, and in many cases the device has to be taken away for servicing with resultant unproductive periods of even several days. For example, the per-

formance of new adjustments often requires that the display device should be opened at a place where the required service equipment is available.

The object of the present invention is to avoid the above disadvantages and to provide a user-friendly system, in which the properties of both the display controller and the display device can be utilized optimally without any need for the user to have any knowledge of their properties, and in which the costs caused by the factory adjustments and the service can be remarkably reduced. This is achieved by means of a method according to the present invention, which is characterized in that a bidirectional data transmission path is established between the display device and the means controlling it so that at least one signal line used for controlling the image displayed by the display device is also utilized in the data transmission mode as the data transmission path. A display system and a display device according to the invention, in turn, are characterized by the features disclosed in the characterizing portions of the attached claims 15, 16 and 17.

The basic idea of the invention is to provide a bi-directional data transmission path between the display device and the means controlling it (the microcomputer and its display controller) so that the data transmission does not require any dedicated signal lines but the data transmission takes place by means of existing signals or signal lines, e.g. such that are otherwise (besides the data transmission mode) used for controlling the image displayed by the display device or for identifying the display device, for instance. The invention enables the display device and the microcomputer to communicate with each other so that they identify each

other while nevertheless keeping to the existing and known device environments as fully as possible.

As the display device and the microcomputer identify each other, the above-mentioned operational problems are eliminated, because the display device is able to inform the display controller and the software controlling it about its compatibility. In this way the possibilities of both the display device and the display controller can always be utilized efficiently without any need for the user to have knowledge about the properties of the devices. The software (which can be supplied on a diskette together with the display device) enables the user of the microcomputer e.g. to align the image to be displayed and to adjust the size, brightness or contrast of the image so that no separate adjusters need to be provided in the display device. In this way the display device will be more advantageous in mechanical structure and electronic arrangement.

In the performance of the factory adjustments, considerable savings in costs are obtained due to a decrease in the amount of manual work, because the adjustments can be performed by means of a system based on the use of a test image and a camera by transmitting the adjustment data through the data transmission path to the display device. As a consequence, no separate connection is needed between the display device and the microcomputer for the factory adjustments, which helps to reduce the costs.

Service becomes more rapid and simpler as the microcomputer may be provided with a test program which requests the display device to show e.g. its own identifier (such as a type number), production version or indication of failure. After the user has run the test program, the service staff can get more

accurate information about the situation by telephone, which facilitates the performance of the service operation at the place where the computer is stationed. To carry out the tests/adjustments, the casing of the display device need not be opened, as the test/adjustment data is transmitted over the data transmission path.

The solution according to the invention also offers a possibility to reduce the power consumption and radiation values of the display device (especially with CRT based display devices) as the microcomputer can switch the display device to various low-power modes.

The preferred and thus the common principle in realizing the invention is to utilize standard solutions as efficiently as possible to avoid extra costs and to maintain complete compatibility with *de facto* standards, such as the VGA display standard. In the embodiment of the invention to be described below, the display controller (microcomputer) requires no new device components (changes in connections), and, if desired, only a few additional components are required for the display device, the resulting additional costs being only a few Finnish marks.

In the following the invention will be described in greater detail with reference to the examples of the attached drawings, in which

Figure 1 is a block diagram illustrating a computer system provided with a display system according to the invention;

Figure 2 is a more detailed view of a connection between a VGA-type display controller and a colour display device for realizing data transmission in accordance with the invention;

Figure 3a illustrates a first embodiment of the level control circuit shown in Figure 2, by means of which data is transmitted from the display device to the microcomputer;

Figure 3b illustrates a second embodiment of the level control circuit shown in Figure 2, by means of which data is transmitted from the display device to the microcomputer;

Figure 4 shows a screen of a CRT based display device and synchronizing signals, illustrating the positioning of the image on the screen by the synchronizing signals in a normal display mode;

Figure 5a is a horizontal timing diagram in a normal display mode;

Figure 5b is a horizontal timing diagram in a data transmission mode according to the invention;

Figure 6 is a timing diagram illustrating the positioning of the data transmission periods in time with respect to the other control signals; and

Figure 7 illustrates the different stages of the method according to the invention in time with respect to the synchronizing pulses.

Figure 1 shows a computer system which may comprise a display system according to the invention. The computer system comprises a central unit (CPU) 1 to which a keyboard 2, a mouse 3 and a display system including a display device 4 are connected. Besides the display device the display system comprises a video display controller 5 which is connected through a bus connection 6 to the central unit (CPU) 1 of the computer. The display controller comprises an image data memory 7 which contains information about the image to be displayed. The display controller 5 generates a video signal VIDEO (which may, as described below, comprise several different physical signals)

which is applied to control the display device 4.

Figure 2 is a more detailed view of a data transmission arrangement between the standard VGA-type display controller 5 and the compatible display device 4. The display controller 5 is connected by means of an interconnecting cable 9 to the display device 4. The signal order of the connector of the display device of the VGA controller complies with the standard as follows:

SIGNAl	NAME	DESCRIPTION
1	R	Analog control signal for red colour. Used only with a colour display device.
2	G	Analog control signal for green colour or for monochrome level. Monochrome-level control is used only with a monochrome display.
3	B	Analog control signal for blue colour. Used only with a colour monitor.
4	ID2	Identification signal for a display device.
5	Reserved	Reserved(grounding)
6	R_Return	Grounding of the red analog signal (pin 1). Used only with a colour monitor.
7	G_Return	Grounding of the green colour or monochrome level signal.

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SIGNAL	NAME	DESCRIPTION
8	B_Return	Grounding of the blue colour. Used only with a colour display device.
9	Key	Coding (the pin hole of the connector blocked).
10	GND	Grounding of digital signals.
11	ID0	Display device identification signal
12	ID1	Display device identification signal
13	HSYNC	Horizontal deflection signal for the display device
14	VSYNC	Vertical deflection signal for the display device
15	Reserved	Reserved

Among these signals, only the control lines 11, 12 and 13 of the red, blue and green colour, the signal lines 14 and 15 of the horizontal and vertical deflection signals HSYNC and VSYNC of the display device, and the signal lines 16 to 18 of the identification signals ID0 to ID2, which are necessary for the understanding of the invention, are shown in Figure 2. The other signal lines are not shown as they are not related to this specific solution.

At the end of the display controller 5, the

arrangement shown in Figure 2 corresponds to a standard VGA arrangement, in which the analog signals (R, G, B) used for the transmission of image information are controlled by means of a VGA control circuit 10, an image data memory 7 (not shown in Figure 2), and an RAMDAC circuit (D/A conversion circuit, colour palette, Colour Look-Up Table, CLUT) 19. As is known, the VGA controller also employs the analog signals to distinguish between the monochrome and colour display devices. This identification is based on the ability of the RAMDAC circuit to supply current, the use of analog signal-level indicators 20, 21 and 22 in the display controller, and the different matching of the R, G and B signals (termination 31, 32) in the monochrome and colour display devices. Only the G signal is connected to the monochrome display device, while all of the three above-mentioned analog signals are connected to the colour display device. Due to the different line matchings of the monochrome and the colour display device, they can be distinguished from each other by supplying a current of a predetermined magnitude by the RAMDAC circuit to all analog signal lines. This causes different voltage levels to occur in the signals R and B as compared with the G signal in the monochrome and colour display devices. The voltage levels of the analog signals are indicated by the level indicators 20 to 22, which indicate whether the device coupled to the display controller is a monochrome display device or a colour display device.

As the display controller 5 shown in Figure 2 corresponds fully to the standard VGA card, its operation will not be described more closely herein. More accurate information about the structure and operation of the card can be found e.g. in Reference

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[1] (the references are listed in the end of the specification).

At the end of the display device 4 (which is a colour display in this example), the arrangement shown in Figure 2 corresponds to the standard display device arrangement with the exception that it further comprises two additional components for realizing a bidirectional data transmission path according to the invention. First, a signal-level control circuit 23 is connected to the G line 12, which control circuit causes a change in the level of the G signal. This change can be detected by means of the level indicator 21 connected to the G line on the side of the display controller. Second, a level indicator 24 is connected to the G line 12 on the side of the display device, which level indicator identifies the changes that the RAMDAC circuit 19 causes in the signal level of the G signal. The output of the level indicator 24 is connected to a serial input 25a in a microcontroller 25 provided in the display device, while the signal-level control circuit is controlled through a serial output 25b of the microcontroller. In practice, the circuit 25 may be any microcontroller or -processor, such as a 8051-type controller (e.g. by Intel).

Figures 3a and 3b show two alternative embodiments for the signal-level control circuit 23. In the alternative of Figure 3a, the control circuit comprises an arrangement connected in parallel with the termination, the arrangement including a termination impedance 27, and a switch 28, by means of which the termination impedance is connected in parallel with a termination resistor 31 provided in the G line. In this way the termination of the G line is changed temporarily, which, in turn, changes temporarily the

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voltage level of the G signal. In the alternative of Figure 3b, the signal-level control circuit 23, in turn, comprises a current generator 29 which is controlled by the microcontroller 25 so as to supply a current control signal to the G line 12. The current control signal changes the voltage level of the G signal, and this change can be detected on the side of the display controller by means of the level indicator 21. In practice, the current generator is easy to realize e.g. by means of a FET and a few resistors.

In the following the data transmission process according to the invention in the equipment shown in Figure 2 will be described in more detail. In the equipment, the signal-level control circuit 23 is the arrangement connected in parallel with the termination, shown in Figure 3a. The starting point is a situation in which the colour display device 4 is controlled by means of the standard VGA display controller 5 of the microcomputer. The following addresses and registers used in the description below are thus standard VGA display controller I/O registers:

3C2 bit 4	= level indicator output 30 inverted, read only register
3C2 bits 7 and 6	= the polarities of the VSYNC and HSYNC signals, write register
3CC bits 7 and 6	= the polarities of the VSYNC and HSYNC signals, read register
3C6	= masking of RAMDAC pixel data
3C7	= read address of RAMDAC
3C8	= write address of RAMDAC
3C9	= RAMDAC data
3BA or 3DA bit 0	= Display enable, read register.

These as well as the other VGA display controller registers are described in more detail in References [2] and [3]. The operating principle and programming of the standard RAMDAC circuit (D/A conversion circuit, CLUT) are described in Reference [4]. In Figure 2, all the signals are indicted with the same references as in Reference [4].

As the present invention relates only to data transmission between a PC and a display device, it is assumed that the display controller 5 has been initialized and the display device 4 has been identified as a colour display device. In the example of Figure 2, however, the data transmission employs only the G signal. Among the R, G and B signals, the G signal is the only one that can be used in data transmission for both a monochrome and a colour display device because only the G signal is used in the monochrome display device.

Transition from the normal display mode to the data transmission mode, actual data transmission, and transition from the data transmission mode back to the display mode take place in stages as follows.

1. Storing the state of the display mode

The data transmission program of the microcomputer stores the state of the display controller 5 before the change of mode. The contents of the registers of the RAMDAC circuit 19 and the VGA controller as well as the contents of the display memory have to be stored in order that it would again be safe to return to the display mode from the data transmission mode.

2. Determining the RAMDAC control parameters

As the display controller is a standard VGA controller, the contents (register address 3C9) of the memory (RAM) of the RAMDAC circuit for each

"colour" may vary between the values 0h and 3Fh (h stands for a hexadecimal value) (cf. Reference [4]). The value 0h minimizes the intensity of the colour in question, while the value 3Fh maximizes it. Due to the inaccuracies of the termination resistors provided in the display devices and the display controllers (resistors 31 and 32 in Figure 2), the safest way is to first search for a G signal control parameter x which causes a change in the output signal 30 of the level indicator 21 of the display controller when the value of the G register of the RAMDAC is increased from the value 0h. The state of the output of the level indicator can be read from the above-mentioned address 3C2, bit 4. The point of change of the output of the level indicator is determined through the steps of:

a. storing the contents of the RAMDAC(0h) (the RAMDAC address 0h is easiest to use as it is addressed continuously when the masking of pixel data (address 3C6) is on);

b. giving the value 0h to the auxiliary variable x,

c. writing the value 0h to the address 3C6 for masking the pixel data,

d. writing the address value 0h to the address 3C8,

e. writing the value 0h to the address 3C9 of the R register of the RAMDAC,

f. writing the value x to the address 3C9 of the G register of the RAMDAC,

g. writing the value 0h to the address 3C9 of the B register of the RAMDAC,

h. increasing the value of x by one; x=x+1,

i. waiting until the image is inactivated (3 DA, bit 0),

j. waiting until the image is activated (3 DA, bit 0),

k. reading the output y=3C2 of the level indicator during the active image,

l. giving y the value y=10h and y, i.e. masking the other bits except for the bit 4,

m. returning to item d, if y=0h,

n. giving x the value x=x+z, i.e. increasing the margin to increase the reliability of the data transmission. The value of the auxiliary variable z depends on the realization of the circuit connected in parallel with the termination,

o. restoring the contents of the RAMDAC(0h).

The above procedure gives the value of x which can be used in the arrangement of Figure 2, in which the level of the G signal is controlled from the display controller by changing the contents of the RAMDAC circuit. As the value of x is known, the RAMDAC circuit is caused to supply a bias current such that it causes the voltage level of the G signal to increase higher than the reference voltage levels of the level indicators 21 and 24. By decreasing the termination impedance of the G signal of the display device, the voltage level produced by the current can be decreased, which, in turn, can be detected by the level indicator of the display controller, that is, the output of the level indicator 21 of the display controller varies between the logical levels 0 and 1 in response to the magnitude of the termination impedance of the display device.

Stage 2 is not necessary; however, it is preferable to carry it out on account of the above-mentioned inaccuracies.

3. Transition to the data transmission mode

Transition to the data transmission mode

according to the invention takes place from a normal display mode in which the synchronization signals position the image on the screen of the display device, as shown in Figure 4. A horizontal deflection period HPER refers to a period during which one horizontal line is scanned from the left to the right and then the beam returns to the start of the next horizontal line. The HPER comprises an active display period H_{active}, which defines a horizontal active image area on the screen and during which the image data read from the image memory is displayed, and a blanking period HBLANK, which comprises at least a front porch HFP, a deflection pulse HSYNC, and a back porch HBP. During the blanking period HBLANK, the electron beam of the cathode ray tube is returned to the start of the next line, for instance. Correspondingly, a vertical deflection period VPER comprises a display period V_{active} and a blanking period VBLANK, which contains at least a front porch VFP, a vertical deflection pulse VSYNC, and a back porch VBP. The display periods H_{active} and V_{active} together define the active image area, which is indicated by the reference B in the figure. HBLANK and VBLANK together determine the time periods during which the BLANK signal is active. The control periods of the vertical deflection consist of the multiples of the horizontal deflection period, the number of the multiples being determined by programmable control parameters.

On transition from the display mode to the data transmission mode, the frequencies, polarities and pulse lengths of the HSYNC and VSYNC signals are changed so that the display device is indicated of the request of the microcomputer to communicate. In addition, the value 00h is written to the I/O address 3C6 of the display controller, as a result of which,

irrespective of the control of the signals P0-P7 (Pixel address) to the RAMDAC circuit, the output of the RAMDAC circuit is dependent only on the contents of the RAMDAC circuit at the address 0h when the control of the BLANK signal to the RAMDAC circuit is not active. Further, x is set in the G register of the RAMDAC (0h) and 0h is set in the R and B registers for generating a bias current required by the data transmission. In order that it would not be necessary to take into account the control of the RAMDAC circuit by the BLANK signal during the data transmission, the position of the BLANK signal is programmed so that it is not active during data transmission (if the BLANK signal controlling the RAMDAC is active, the levels of the R, G and B signals of the RAMDAC are at a minimum). Figures 5a and 5b illustrate the changes caused by the transition in the horizontal timing diagram. Figure 5a represents a normal display mode (cf. Figure 4), i.e. the image is displayed within an area A1 where the BLANK signal is not active. In Figure 5b, transition to the data transmission mode has taken place, and so the length of an active portion A2 of the BLANK signal (the BLANK signal is active when it is "low", that is, in the logical stage 0) is minimized, and it has been displaced farther away from the HSYNC pulses.

In VGA display controllers, the positions of the BLANK, VSYNC, and HSYNC signals can be programmed relatively freely, whereas in display controllers where the BLANK signal is not programmable it has to be ensured by software that the output(s) of the level indicators(s) is(are) read only during the active image.

4. Data transmission

4.1. The display device detects the data transmission mode by monitoring the VSYNC and the HSYNC signals. By means of the level indicator 24 the display device also detects that the G signal is controlled by the display controller 5. The display device prevents the propagation of the R, G and B signals to the video amplifier so as to minimize the disturbances on the screen.

4.2. The display device waits for the following VSYNC period and acknowledges the detection of the data transmission mode. This takes place so that the microcontroller 25 activates the switch 28, and so the termination impedance 27 is connected in parallel with the termination resistor 31. This causes a change in the voltage level of the G signal (the level drops below the reference level of the level indicator 21).

4.3. The microcomputer waits for the VSYNC signal (as the acknowledgement of the display device is synchronized with the VSYNC signal) and reads the state of the output of the level indicator 21 of the display controller. If the microcomputer detects a change in the state of the output, it knows that the display device is capable of data transmission. As the display device does not activate the parallel connection immediately (the display device needs a few VSYNC periods for the identification of the data transmission mode), the microcomputer has to check several times whether the display device is capable of data transmission or not. If the display device is capable of data transmission, the procedure is continued from item 4.4., otherwise skip to item 4.9.

4.4. The display waits for the VSYNC signal (at this stage two VSYNC pulses have elapsed from the

activation of the parallel connection of the G signal, and so there is one complete field period during which the microcomputer can detect the acknowledgement of the display device) and reopens the switch 28, thus disabling the parallel connection.

4.5. The microcomputer waits for the cancellation of the acknowledgement.

4.6. The microcomputer writes either the value x or the value 0h in the G register of the RAMDAC(0h) of the display controller in synchronization with the HSYNC pulses, whereby, however, the first control is 0h, which is also a start bit for the display device. The display device reads the controls of the display controller in synchronization with the HSYNC pulses by using its own level indicator 24 (the reading takes place in the horizontal timing diagram within areas A3 indicated in Figure 5b). The interpretation of the controls and the allowable duration of the controls during one field period depend on the specifications of the data transmission protocol and the set data transmission mode. As already mentioned above, data transmission cannot be performed while the BLANK signal is active.

Figure 6 illustrates data transmission within areas A4 with interruptions during the blanking periods HBLANK and VBLANK.

Acknowledgement and responding take place as follows:

4.7. The microcomputer writes x in the G register of the RAMDAC(0h) of the display controller.

4.8. The display device waits for the VSYNC signal and starts to control the circuit 23 parallel with of the termination in synchronization with the HSYNC signal, thus causing corresponding voltage variation in the G signal. This is detected by means

of the level indicator 21 of the display controller. The start bit (0) is again transmitted first, and then the other bits.

The microcomputer reads the level indicator 21 of the display controller in synchronization with the HSYNC signal and interprets the message it receives. Changes in the direction of data transmission can be determined by means of the protocol applied in the transmission.

4.9a. After the transmission of all controls/commands, the data transmission is terminated in such a way that the display controller restores the display mode by restoring the VGA and RAMDAC registers and the display memory to the state which the controller stored at the stage 1, i.e. to the state in which they were immediately before the transition to the data transmission mode.

4.9b. The display device detects the change in the mode of operation on the basis of the changed frequencies, polarities and pulse lengths of the HSYNC and VSYNC signals, and so it returns to the normal display mode according to Figure 4.

Figure 7 shows the above-described steps as a timing diagram with the data transmission taking place during step 4.6 spread out. As data is transmitted in synchronization with the HSYNC pulses, it is possible to transmit one byte during 12 horizontal lines, the byte comprising a start bit, eight data bits D0-D7, a parity bit P and two stop bits. In this way the transmission rate of the transmission path according to the invention will correspond to the data transmission rate of a rapid modem.

In the above example, the method according to the invention has been described in a so-called half duplex mode, in which the data transmission takes

place alternately in opposite directions of transmission. The method can also be easily modified for a so-called full duplex mode, in which the data transmission takes place simultaneously in both directions of transmission. In the following the modifications required for transition from the half duplex mode to the full duplex mode will be described.

The full duplex mode differs from the half duplex mode mainly in that two signal lines are used simultaneously in the data transmission. The common reference level of the level indicators 20 to 22 thereby deviates from the reference level of the level indicator 24. The common reference level of the level indicators 20 to 22 is still VGA compatible, whereas the reference level of the level indicator 24 deviates substantially from it, being either below or above the reference level of the level indicators 20 to 22. In the following, it is assumed that the G and R lines are used in the data transmission, and that the reference level of the level indicator 24 is lower than that of the level indicators 20 to 22. When the signal of the G line is controlled, the level indicator 24 already applies a voltage change signal to a serial input 25a of the microcontroller 25 when the level indicator 21 does not yet identify the voltage level. The RAMDAC circuit of the display controller maintains the biasing level of the video signal R throughout the communication stage, and the microcontroller 25 controls the R signal by means of the signal-level control circuit 23. As the control levels of the G signal are clearly below those of the R signal, variations in the G signal do not cause changes in the state of the output signal 30 of the level indicators 20 to 22. Only the variations caused in the R signal by the microcontroller by means of

the control circuit 23 cause changes in the output signal 30.

In other respects the full duplex mode corresponds essentially to the above-described half duplex mode. Only the criteria for selecting the control parameters of the RAMDAC circuit are different (due to the differences described above). In the full duplex mode of operation, the direction of data transmission need not be taken into account in the data transmission protocol, as distinct from the half duplex mode. The full duplex mode is, however, optimally suited for use with a colour display device only, as only one video signal line is available in the monochrome display device. Therefore the half duplex mode has a wider range of applications than the full duplex mode.

Even though it is most advantageous in the full duplex mode that the signal lines used in the transmission of video information are used as signal lines, it is, in principle, possible to select two signal lines more generally from the following groups, either from the same group or from different groups:

- the signal lines 11, 12 and 13 of the analog signals R, G and B,
- the signal lines 14 and 15 of the deflection signals HSYNC and VSYNC,
- other signal lines used for the control of the image displayed by the display device (such as dotclk, display_enable, etc.), and
- the signal lines 16 to 18 of the identification signals ID0, ID1 and ID2.

The solution according to the invention can be used with any display device controllable by a video signal. Such a display device may be e.g. a cathode

ray tube display, liquid crystal display, electroluminance display, a plasma display, etc. Interfaces with different signal orders, different connectors, or different signals used in the interfaces, for example, do not either impose any limitations.

For a display device possessing no "intelligence" (no microcontroller or -processor), a simple impulse/response based embodiment of the method according to the invention can be used. In this embodiment the display control means transmit a predetermined deflection signal control (impulse) to the display device, which identifies the control and returns an acknowledgement of the identification (response). The deflection signal control is defined as predetermined frequencies, pulse lengths, polarities, etc., and different controls may be defined for different display devices.

If one or more video signal lines are to be used as the data transmission path, as in the example above, the line(s) can be controlled from the display controller not only by changing the contents of the RAMDAC circuit but also in other ways. For example, the control may be carried out e.g. by altering the contents of the image data memory 7, by controlling the video signal directly by a display controller circuit 10 or by utilizing an overlay function available in certain RAMDAC memories.

From the signals used for controlling the image displayed by the display device outside the data transmission mode, the deflection signals HSYNC and VSYNC, for instance, can also be used for the communication purposes. The deflection signals are controlled directly by the display controller circuit or they are multiplexed with the signals of the display controller circuit. The display device also

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directly controls the deflection signals, which are read on the side of the display controller by software. As standard display controller arrangements do not enable a direct control of the deflection signals, this embodiment requires changes in the display controller, and so it is less advantageous than the example described above, which does not require any changes in the connections of the display controller.

In addition to the analog signals and deflection signals used for the transmission of the actual image information, the other signals used for the control of the image displayed by the display device outside the data transmission mode can also be used for the communication purposes, such as the video clock signal or the Video_Enable signal. The video clock signal might be especially useful in portable microcomputers comprising no CRT-based display. These embodiments, however, also require changes in existing display controllers.

On the contrary, if the identification signals are used for the communication, they are controlled, similarly as the deflection signals, directly by means of the display controller circuit, or multiplexed with the signals of the display controller circuit. The display device also controls directly the identification signals, which are read from the side of the display controller by software. As all display controller arrangements do not comprise any identification signal connections, this embodiment is not as advantageous as the above-described example.

All the above-described signals may also be combined in an appropriate way.

A suitable communication protocol may also be

used between the microcomputer and the display device. This arrangement, however, requires a display device of a more complex structure, as the protocol requires intelligence from the display device. The arrangement may be carried out by a microprocessor, a microcontroller or a logic connection.

The communication may also be effected during the conventional use of the microcomputer so that the user does not notice it in any way. The communication thereby has to be carried out outside the screen area. When identification signals are used, the data transmission can be effected during the active image area without that the user notices it in any way.

Even though the invention has been described above with reference to the examples of the attached drawings, it is obvious that the invention is not restricted to them, but it can be modified in various ways within the scope of the inventive idea disclosed in the above description and in the attached claims.

References:

[1] Programmer's Guide to PC & PS/2 Video Systems, Richard Wilton, Microsoft Press, 1987.

[2] IBM Personal System/2™ Display Adapter, Technical Reference, 68X2251, S68X-2251-0, April 1987.

[3] IBM Personal System/2™ Model 80, Technical Reference.

[4] IMS G171 High Performance CMOS Colour Look-up Table, the Graphics Databook, Inmos, June 1990.

Claims:

1. A method for controlling a display device (4) in a display system by means of display control means (5, 1), wherein

- data concerning the display device is transmitted from the display device (4) to the display control means (5, 1), and

- image control data is transmitted from the display control means (5, 1) to the display device (4) for controlling an image displayed by the display device, characterized in that a bi-directional data transmission path is established between the display device (4) and the means (5, 1) controlling it so that at least one signal line (12; G) used for controlling the image displayed by the display device (4) is also utilized in the data transmission mode as the data transmission path.

2. A method according to claim 1, characterized in that at least one signal line (11, 12, 13) used in the transmission of video information is utilized as the data transmission path.

3. A method according to claim 2, characterized in that said at least one video signal line is controlled from the display control means (5, 1) by changing the contents of the memory of a D/A conversion circuit (RAMDAC) (19).

4. A method according to claim 2, characterized in that said at least one video signal line is controlled from the display control means (5, 1) by a display controller circuit (10) directly.

5. A method according to claim 2, characterized in that said at least one video signal line is controlled from the display control means (5, 1) by changing the contents of an image data memory

(7).

6. A method according to claim 2, c h a r a c t e r i z e d in that the transmission and/or reception of data is synchronized by means of at least one deflection signal (HSYNC, VSYNC).

7. A method according to claim 1 or 2, c h a r a c t e r i z e d in that at least two signal lines are utilized as the data transmission path, and that data can be transmitted simultaneously in both directions.

8. A method according to claim 1, c h a r a c t e r i z e d in that transition from the normal display mode to the data transmission mode is carried out by means of an impulse applied to the display device (4) by changing the parameters, such as frequency, polarity and pulse length, of at least one deflection signal (HSYNC, VSYNC) to predetermined values.

9. A method according to claim 8, c h a r a c t e r i z e d in that the whole data transmission is carried out as a simple identification procedure by means of said impulse and a response produced to it by the display device (4).

10. A method according to claim 1, c h a r a c t e r i z e d in that at least data about the properties or state of the display device (4) is transmitted during the data transmission mode from the display device (4) to the display control means (5, 1).

11. A method according to claim 1, c h a r a c t e r i z e d in that at least test/adjustment data is transmitted during the data transmission mode from the display control means (5, 1) to the display device (4).

12. A method for controlling a display device

(4) in a display system by means of display control means (5, 1), wherein

- data concerning the display device is transmitted from the display device (4) to the display control means (5, 1), and

- image control data is transmitted from the display control means (5, 1) to the display device (4) for controlling an image displayed by the display device, characterized in that a bi-directional data transmission path is established between the display device (4) and the means (5, 1) controlling it so that at least one signal line (16 to 18) used for identifying the display device (4) is also utilized in the data transmission mode as the data transmission path.

13. A method according to claim 12, characterized in that at least two signal lines are utilized as the transmission path, and that the data transmission takes place in both directions simultaneously.

14. A method according to claim 12, characterized in that said at least one signal line (16 to 18) is controlled from the display control means (5, 1) directly by means of a display controller circuit (10).

15. A display system comprising a display device (4) and display control means (5, 1) controlling the display device (4) and connected to it by means of at least one signal line (12) intended for controlling an image displayed by the display device, characterized in that a bi-directional data transmission path is established between the display device (4) and the display control means (5, 1), the data transmission path comprising at least one signal line (12) intended for

controlling an image displayed by the display device (4).

16. A display system comprising a display device (4) and display control means (5, 1) controlling the display device (4) and connected to it by means of at least one signal line (12) intended for controlling an image displayed by the display device (4), and at least one signal line (16 to 18) used for identifying the display device, c h a r a c t e r i z e d in that a bidirectional data transmission path is established between the display device (4) and the display control means (5, 1), the data transmission path comprising at least one of said signal lines (16 to 18) used for the identification of the display device (4).

17. A display device (4) comprising at least one incoming signal line (12) from the display control means (5, 1), the incoming signal line being used for the transmission of image data, c h a r a c t e r i z e d in that the display device comprises means (23) for changing the signal level of said signal line (12), and a level indicator (24) for detecting changes in the signal level from the display control means (5, 1).

18. A display device according to claim 17, c h a r a c t e r i z e d in that the means (23) for changing the signal level comprise means (27, 28) for changing the termination of said signal line (12) temporarily.

19. A display device according to claim 17, c h a r a c t e r i z e d in that the means (23) for changing the signal level comprise means (29) for applying a current control signal to said signal line (12).

AMENDED CLAIMS

[received by the International Bureau
on 1 February 1993 (01.02.93);
original claim 17 amended; other claims unchanged (5 pages)]

1. A method for controlling a display device (4) in a display system by means of display control means (5, 1), wherein

- data concerning the display device is transmitted from the display device (4) to the display control means (5, 1), and

- image control data is transmitted from the display control means (5, 1) to the display device (4) for controlling an image displayed by the display device, c h a r a c t e r i z e d in that a bi-directional data transmission path is established between the display device (4) and the means (5, 1) controlling it so that at least one signal line (12; G) used for controlling the image displayed by the display device (4) is also utilized in the data transmission mode as the data transmission path.

2. A method according to claim 1, c h a r a c t e r i z e d in that at least one signal line (11, 12, 13) used in the transmission of video information is utilized as the data transmission path.

3. A method according to claim 2, c h a r a c t e r i z e d in that said at least one video signal line is controlled from the display control means (5, 1) by changing the contents of the memory of a D/A conversion circuit (RAMDAC) (19).

4. A method according to claim 2, c h a r a c t e r i z e d in that said at least one video signal line is controlled from the display control means (5, 1) by a display controller circuit (10) directly.

5. A method according to claim 2, c h a r a c t e r i z e d in that said at least one video signal line is controlled from the display control means (5, 1) by changing the contents of an image data memory

(7).

6. A method according to claim 2, c h a r a c - t e r i z e d in that the transmission and/or reception of data is synchronized by means of at least one deflection signal (HSYNC, VSYNC).

7. A method according to claim 1 or 2, c h a r - a c t e r i z e d in that at least two signal lines are utilized as the data transmission path, and that data can be transmitted simultaneously in both directions.

8. A method according to claim 1, c h a r a c - t e r i z e d in that transition from the normal display mode to the data transmission mode is carried out by means of an impulse applied to the display device (4) by changing the parameters, such as frequency, polarity and pulse length, of at least one deflection signal (HSYNC, VSYNC) to predetermined values.

9. A method according to claim 8, c h a r a c - t e r i z e d in that the whole data transmission is carried out as a simple identification procedure by means of said impulse and a response produced to it by the display device (4).

10. A method according to claim 1, c h a r - a c t e r i z e d in that at least data about the properties or state of the display device (4) is transmitted during the data transmission mode from the display device (4) to the display control means (5, 1).

11. A method according to claim 1, c h a r a c- t e r i z e d in that at least test/adjustment data is transmitted during the data transmission mode from the display control means (5, 1) to the display device (4).

12. A method for controlling a display device

(4) in a display system by means of display control means (5, 1), wherein

- data concerning the display device is transmitted from the display device (4) to the display control means (5, 1), and

- image control data is transmitted from the display control means (5, 1) to the display device (4) for controlling an image displayed by the display device, c h a r a c t e r i z e d in that a bi-directional data transmission path is established between the display device (4) and the means (5, 1) controlling it so that at least one signal line (16 to 18) used for identifying the display device (4) is also utilized in the data transmission mode as the data transmission path.

13. A method according to claim 12, c h a r a c t e r i z e d in that at least two signal lines are utilized as the transmission path, and that the data transmission takes place in both directions simultaneously.

14. A method according to claim 12, c h a r a c t e r i z e d in that said at least one signal line (16 to 18) is controlled from the display control means (5, 1) directly by means of a display controller circuit (10).

15. A display system comprising a display device (4) and display control means (5, 1) controlling the display device (4) and connected to it by means of at least one signal line (12) intended for controlling an image displayed by the display device, c h a r a c t e r i z e d in that a bi-directional data transmission path is established between the display device (4) and the display control means (5, 1), the data transmission path comprising at least one signal line (12) intended for

controlling an image displayed by the display device (4).

16. A display system comprising a display device (4) and display control means (5, 1) controlling the display device (4) and connected to it by means of at least one signal line (12) intended for controlling an image displayed by the display device (4), and at least one signal line (16 to 18) used for identifying the display device, c h a r a c t e r i z e d in that a bidirectional data transmission path is established between the display device (4) and the display control means (5, 1), the data transmission path comprising at least one of said signal lines (16 to 18) used for the identification of the display device (4).

17. A display device (4) comprising a screen for displaying visual information to the user, and at least one incoming signal line (12) from the display control means (5, 1), the incoming signal line being used for the transmission of image data, c h a r a c t e r i z e d in that the display device comprises means (23) for changing the signal level of said signal line (12).

18. A display device according to claim 17, c h a r a c t e r i z e d in that the means (23) for changing the signal level comprise means (27, 28) for changing the termination of said signal line (12) temporarily.

19. A display device according to claim 17, c h a r a c t e r i z e d in that the means (23) for changing the signal level comprise means (29) for applying a current control signal to said signal line (12).

20. A display device according to claim 17, c h a r a c t e r i z e d in that it further com-

prises a level indicator (24) for detecting changes in the signal level from the display control means (5, 1).

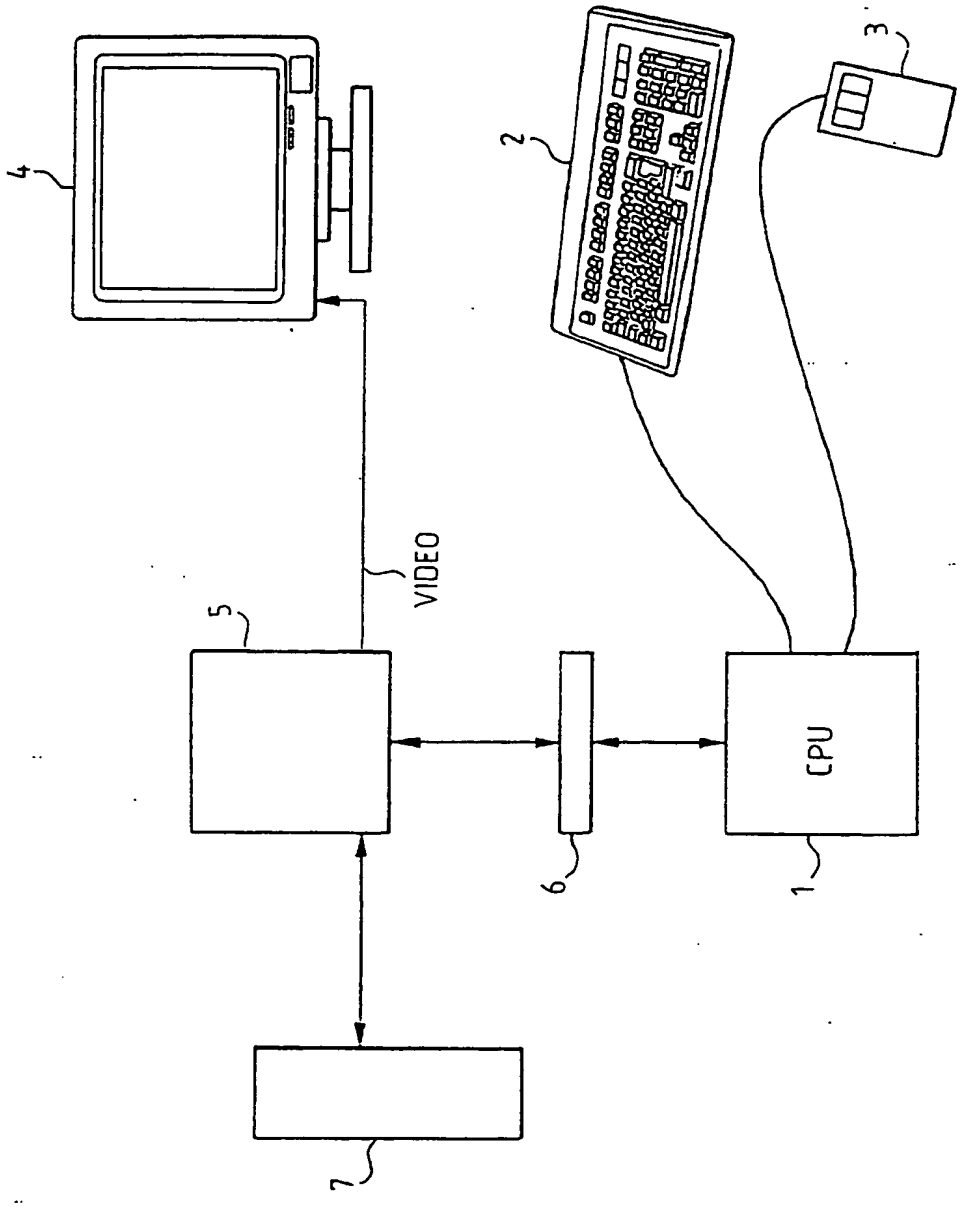
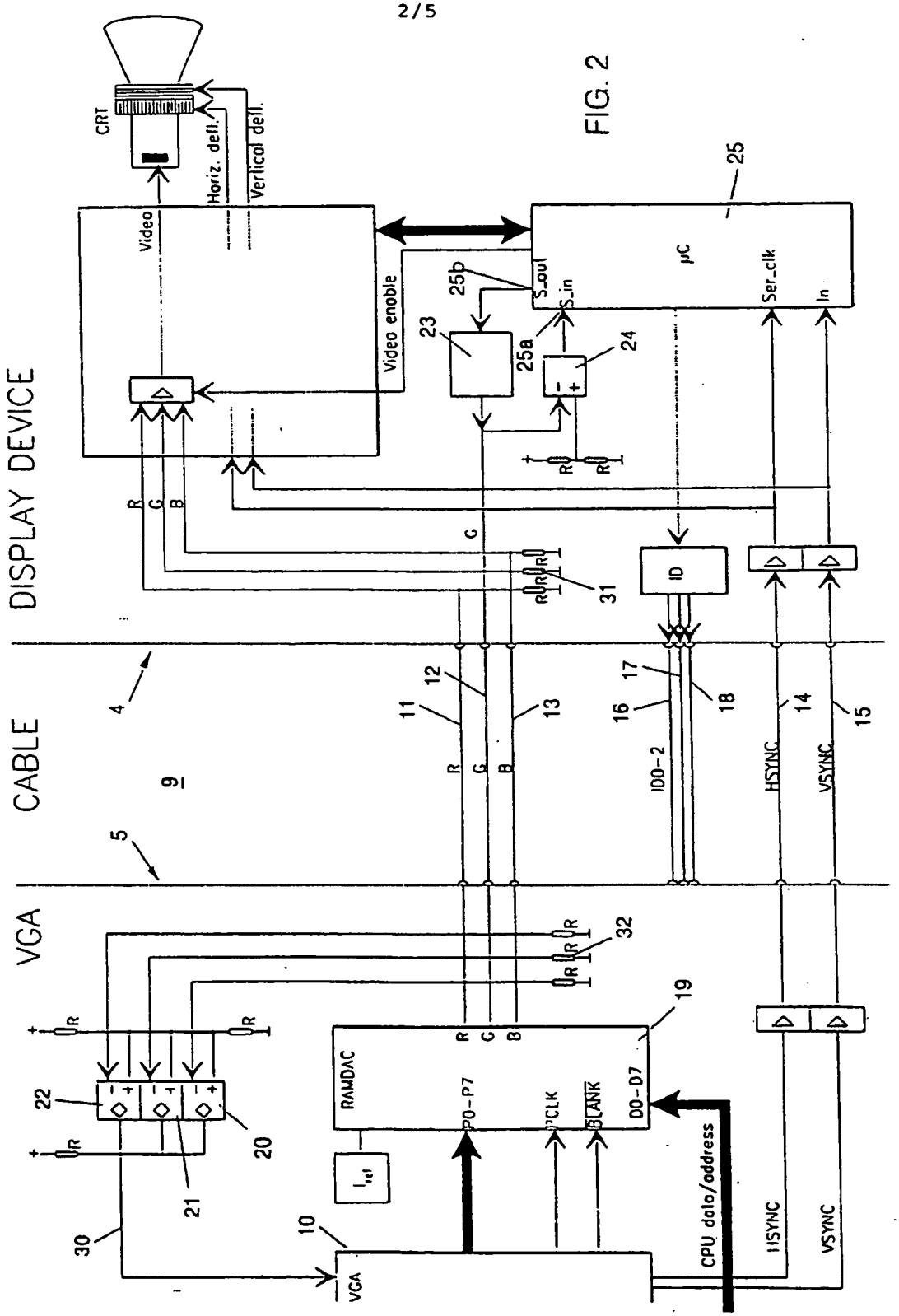


FIG. 1

FIG. 2


DISPLAY DEVICE
CABLE
VGA
CRT
Horiz. defl.
Vertical defl.
Video
Video enable
μC
Ser_clk
In
S_out
S_in
25
25b
25a
23
24
31
ID
4
9
5
12
11
13
17
16
18
14
15
IDO-2
HSYNC
VSYNC
32
19
22
20
21
30
10
RAMDAC
PO-P7
CLK
BLANK
DO-D7
CPU data/address
HSYNC
VSYNC
VGA

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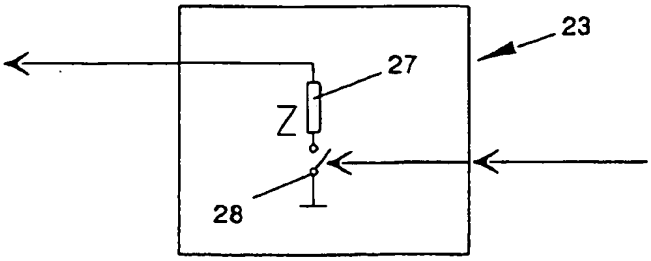

FIG. 3a

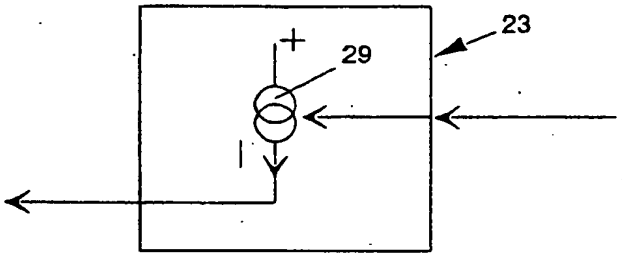

FIG. 3b

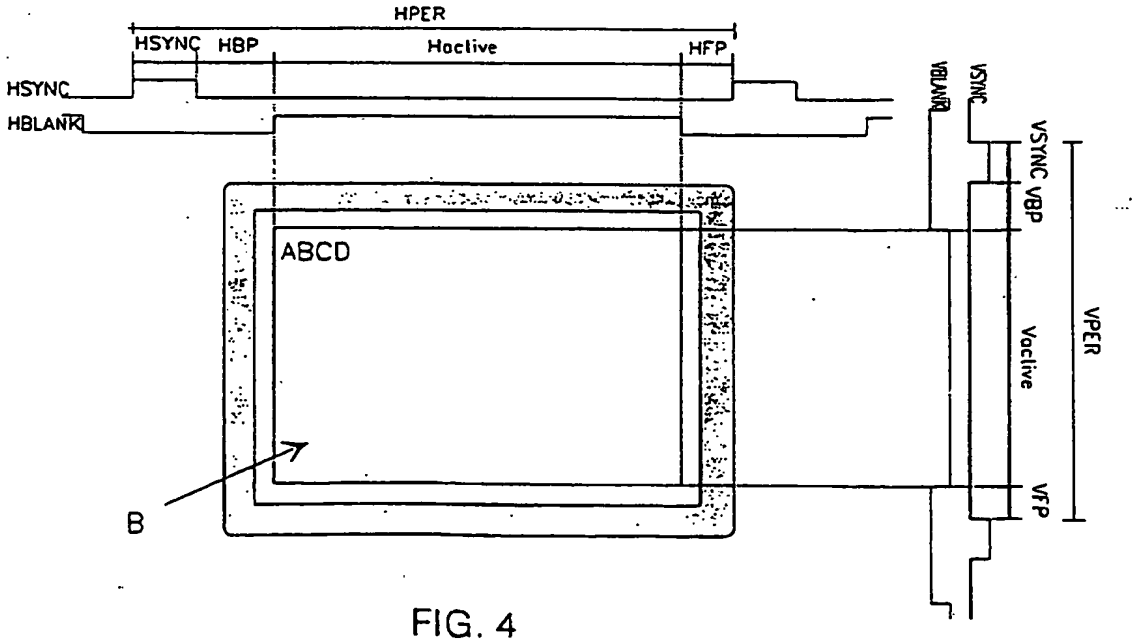

FIG. 4

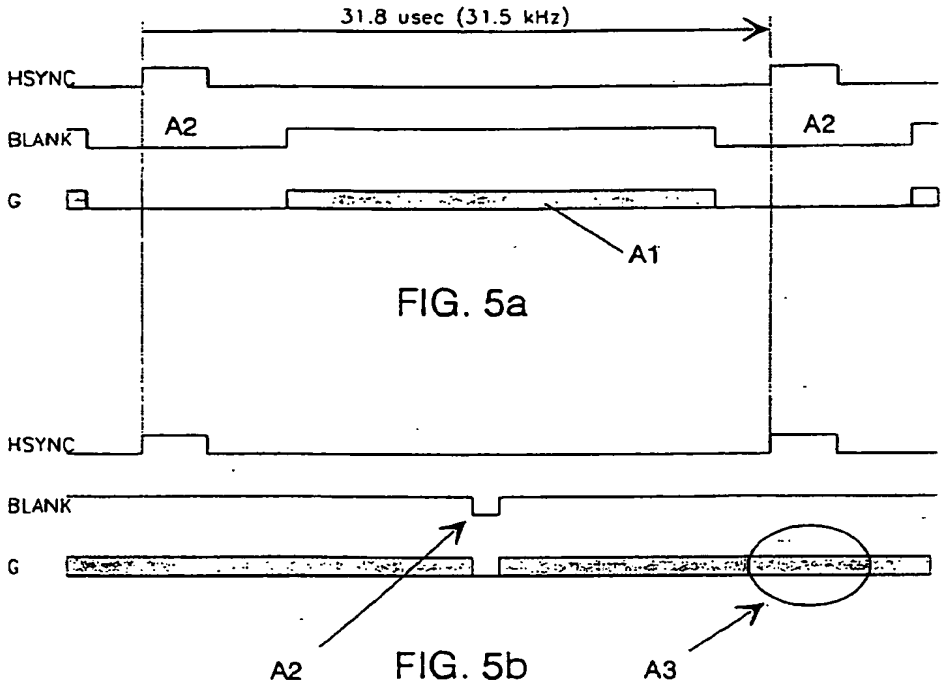

FIG. 5a

FIG. 5b

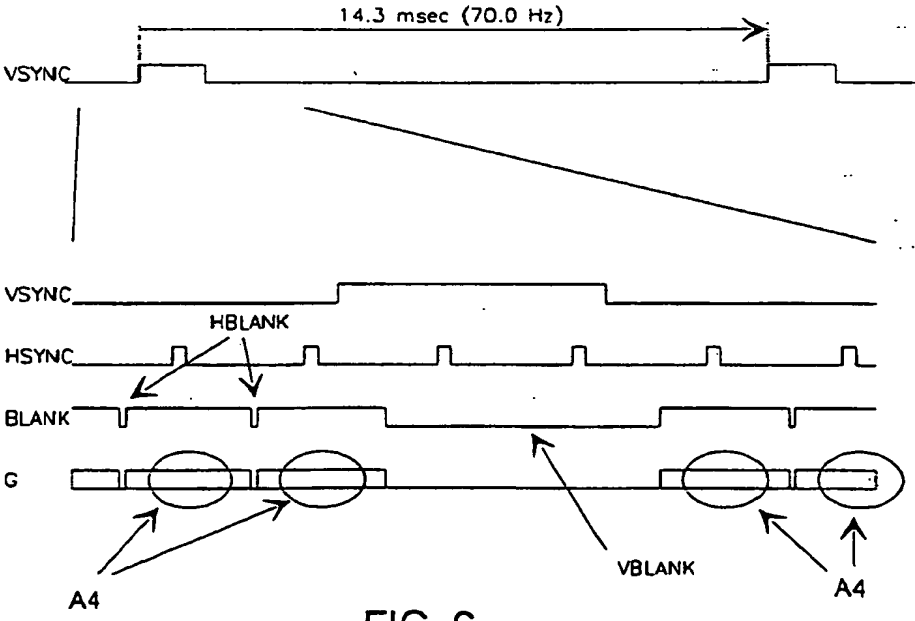

FIG. 6

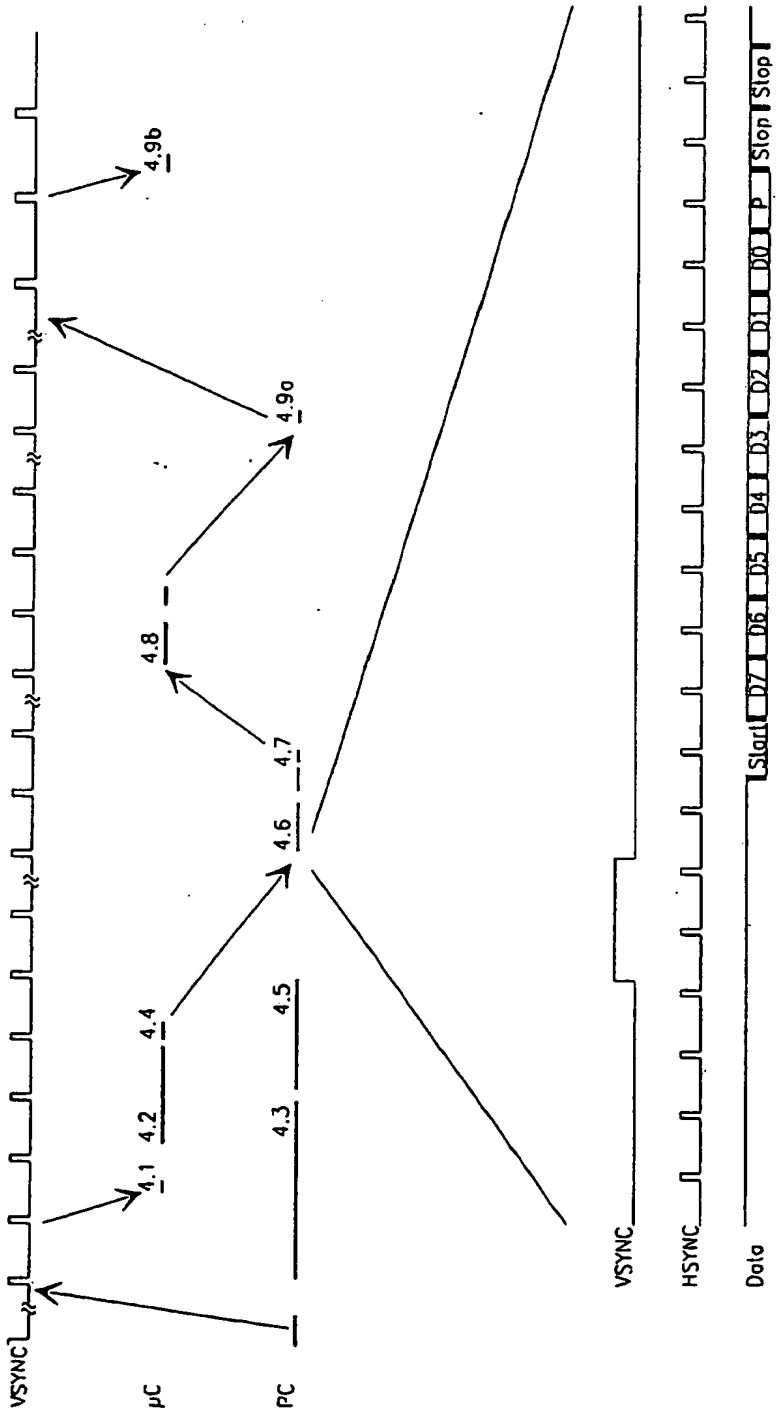
VSYNC
μC
PC
4.1
4.2
4.3
4.4
4.5
4.6
4.7
4.8
4.9a
4.9b
VSYNC
HSYNC
Data
Start
D7
D6
D5
D4
D3
D2
D1
D0
P
Stop
Stop

FIG. 7

INTERNATIONAL SEARCH REPORT

International Application No PCT/FI 92/00244

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all)[6]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC5: G 09 G 5/00

II. FIELDS SEARCHED

Minimum Documentation Searched[7]

Classification System	Classification Symbols
IPC5	G 09 G, G 06 F

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in Fields Searched[8]

SE,DK,FI,NO classes as above

III. DOCUMENTS CONSIDERED TO BE RELEVANT[9]

Category *	Citation of Document,[11] with indication, where appropriate, of the relevant passages[12]	Relevant to Claim No.[13]
A	EP, A2, 0170816 (INTERNATIONAL BUSINESS MACHINES CORPORATION) 12 February 1986, see the whole document	1-19

* Special categories of cited documents: [10]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
16th December 1992	22-12-1992
International Searching Authority	**Signature of Authorized Officer**
SWEDISH PATENT OFFICE	JAN SILFVERLING

Form PCT/ISA/210 (second sheet) (January 1985)

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON INTERNATIONAL PATENT APPLICATION NO.PCT/FI 92/00244

This annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The members are as contained in the Swedish Patent Office EDP file on 02/12/92
The Swedish Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent document cited in search report	Publication date	Patent family member(s)		Publication date
EP-A2- 0170816	86-02-12	AU-D-	4254985	86-01-23
		CA-A-	1235537	88-04-19
		DE-A-	3584403	91-11-21
		GB-A-B-	2162026	86-01-22
		JP-B-	3055833	91-08-26
		JP-A-	61027585	86-02-07
		US-E-	RE33916	92-05-05
		US-A-	4727362	88-02-23